25.9 A Cryogenic ADC operating Down to 4.2K

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Low-temperature detectors for X-ray and far-IR imaging and spectroscopy for space exploration and particle experiments require proximity electronics also cooled to deep cryogenic temperatures, typically below 10K [1]. These cryogenic readout electronic circuits are single-ended pre-amplifiers (JFET or CMOS based) and analog multiplexers, of which the analog output signals are transported towards "warm" or room-temperature (RT) ADCs and signal-processing electronics. Cryogenic ADCs would improve signal integrity between cold and warm electronics. At present, the only ADCs operational at cryogenic temperatures mentioned in literature, are superconductive circuits (Josephson junctions) [2], whose working temperature is limited to a maximum temperature of 10K. Warm testing of the detector system is hence impossible. A cryogenic ADC, operating from room temperature (at the start of the cooling process) down to below 10K would overcome this problem.

The absence of ADCs operating at deep cryogenic temperatures is due to the phenomenon of carrier freeze out in most semiconductor technologies at such low temperatures. Contrary to circuits cooled down to 77K, where the performance of CMOS circuits enhances (due to lower leakage current, improved mobility and decreased thermal noise), at temperatures below 77K and especially below 10K several low-temperature-induced abnormalities occur. The most prominently visible irregularities in the IV characteristic are the negative transconductance region located at the transition linear-saturation with clockwise hysteresis, the associated current overshoot in the time domain, and the kink at V_{DS} mid-supply with counterclockwise hysteresis. In Fig. 25.9.1, a typical IV characteristic for an NMOS transistor at 4.2K is shown. These phenomena deteriorate the behavior of, or even completely disable, classic analog building blocks.

Although currently most cryogenic effects are physically explained [3], no SPICE-applicable below carrier-freeze-out temperature models are available. Hence cryogenic CMOS electronics were up to now designed in a quasi-empirical way. Circuits with some complexity have not yet been reported.

Key factors to cryogenic CMOS design are proper biasing and switching schemes in order to minimize the influence of the cryo-effects mentioned above. Applying these techniques, a CMOS ADC functional between ambient temperature and 4.2K is designed using a conventional CMOS process. Moreover, its low-temperature behavior can be simulated and predicted with adequate precision with SPICE, using parameters extracted from cryogenic transistors measurements. The test chip of this paper, is the result of a single run. No design iterations are necessary.

The ADC architecture is a SAR ADC architecture. It consists of a capacitive DAC, a charge-transfer pre-amplifier (CTA) [4], a latched comparator, and an externally settable SAR. All building blocks are adapted to and optimized for low temperatures, but are also functional at room temperature. The detailed schematic is shown in Fig. 25.9.2. Since cryogenic temperatures do not considerably affect the performance of digital building blocks, most of the design considerations are focused on the analog building blocks described below. The digital gates are implemented with cascode structures.

The comparator [5,6] has a PMOS input, as p-type transistors are less affected by cryogenic temperatures than n-type transistors. As the matching of the transistor pairs degrades with temperature, a pre-amplifier is necessary to optimize the overall system offset and consequently the accuracy of the ADC.

A fully differential CTA architecture [4] is selected as a pre-amplifier, not only because of its robustness to technology variations, or low power consumption, but the CTA preceded by a binary-weighted capacitive DAC, allows to control the voltages at the terminals of the NMOS at cryogenic temperatures (Fig. 25.9.3). Hence the transistors will be brought to a biasing point in its saturation region during the pre-charge phase. Therefore, no negative transconductance will occur in the NMOS transistor during the following amplification phase.

To improve the accuracy of the ADC, the layout of the capacitors banks needs to be balanced out (e.g., common centroid) as other post-processing trimming techniques as laser trimming are not possible at cryogenic temperatures for practical reasons.

An 8b ADC is implemented in a conventional 0.7µm CMOS technology. Tests are performed both at room temperature as well as at 4.2K (LHT). Sampling rate is 3kHz, which is suited for various low-temperature space-observation applications. The power consumption is 350µW from a 5V supply for a load capacitance of 300pF (Fig. 25.9.5).

While cooling the ADC from ambient temperature down to 4.2K, no instabilities or hysteresis induced by the low temperature are observed. The INL increases from 0.5 to -0.8 LSB and the DNL from 0.4 to 1.1LSB.

Acknowledgments:
Authors want to thank J. Putzeys and T. Souverijns for their helpful discussions and support during lab evaluations.

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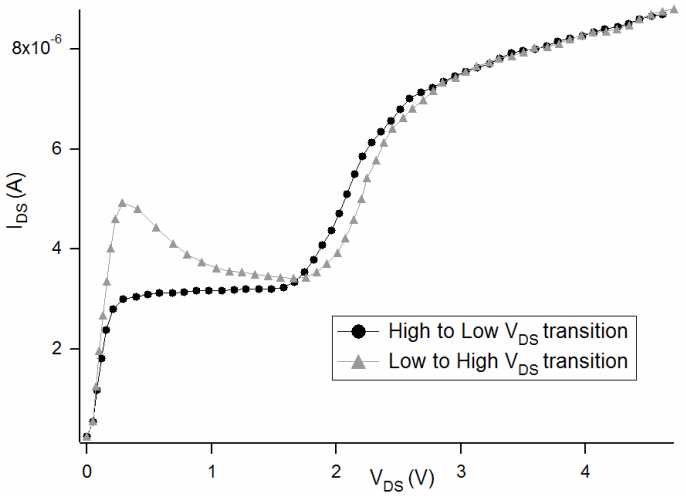

Figure 25.9.1: IV behaviour of a standard 0.7µm NMOS at 4.2K.

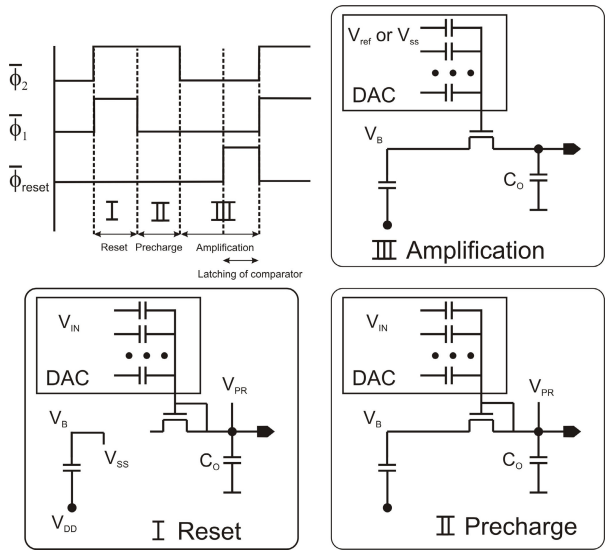

Figure 25.9.3: Switching scheme of the CTA.

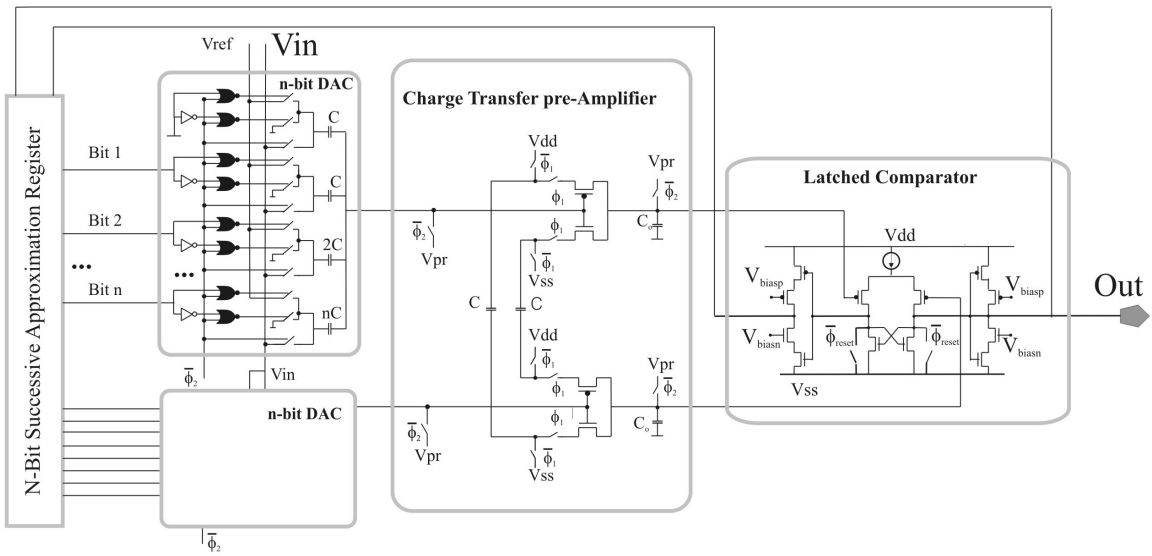

Figure 25.9.2: Successive-approximation ADC architecture for low temperature.

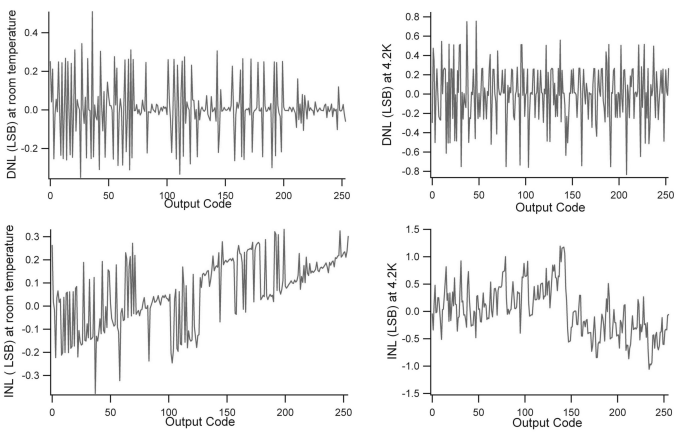

Figure 25.9.4: DNL (top) and INL (below) measurements at room temperature (left) and 4.2K (right).

Technology	0.7µm CMOS 1P2M processed by AMIS	
Supply Voltage	5V	
External output capacitance	300pF	
Power consumption	350µW	
Input Range	5V	
Sampling frequency	3kHz	
	T = 4.2K	**T = 293K**
DNL	-0.8 LSB	0.5 LSB
INL	1.1 LSB	0.4 LSB

Figure 25.9.5: Measured performance summary.

Continued on Page 616

25

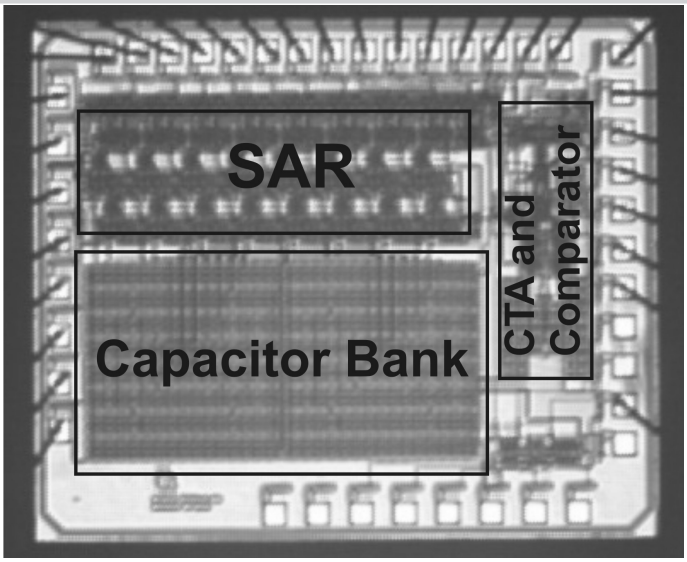

Figure 25.9.6: Die micrograph.

